A 3D Stacked Programmable Image Processing Engine in a 40nm Logic Process with a Detector Array in a 45nm CMOS Image Sensor Technologies

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Abstract Current mobile camera systems present a huge image signal processing (ISP) programmable limitation, since the ISP algorithm is mainly hard-coded via Application Processor. We'll present the prototype development result of a Re-Configurable Instruction Cell Array (RICA), a real time, and low power reprogrammable ISP engine stacked with 8MP detector array in 45nm BSI CMOS imager, and 40nm logic technologies. We believe this RICA stacked image sensor technology presents an efficient programmability solution to support adjacent IOT markets, and next generation computational camera technologies.

1. Introduction

When mobile camera stormed into the mass market, and totally changed the way we communicating, sharing photos/videos, and engaging social events, the mobile camera system consists of discreted optics & sensor, but with integrated processing/multi-function system. This camera path offers compact system solution with fewer custom parts. Although this approach is still facing complex tuning, it represents a mature solution.

As the paradigm shift toward mobile computational photography, it's essential to migrate from the discrete camera systems into integrated imaging and digital optics, to compensate computationally of technology limitations. Therefore, the concept of computational camera consists of integrated optics, integrated sensor, processing, multifunction system, which offers a fully integrated system solution with complex image tuning replaced by software programmability.

It has become apparent that the Next-Gen of camera systems will be computational, and closed coupled to optics & processing. Even today the variety of available image sensor technologies make programmable architectures the preferred solution. A Reconfigurable Instruction Cell Array (RICA) [1] has been developed with an architecture aimed at high speed data-streaming applications. This processing architecture is suitable as reconfigurable image and video core. It offers the configurability of an FPGA, the programmability of a DSP, and at the same time the speed of hardwired solutions. With the availability of stacked image sensor technologies, it presents an opportunity to insert RICA into the stacked sensor implementation.

2. Device Formation

We have designed & fabricated a RICA ASIC wafer stacked with a pixel arrays wafer of 8MP, 1.1 um pitch BSI image sensor with low noise readout as the test vehicle, as illustrated in Fig-1. This device take advantage of the matured 3D stacking technologies [2] of a 45nm CIS process and a 40nm logic process at TSMC. The pixel architecture adopts a 2x2-shared to gain pixel cell utilization of photo-detector. Design of the low readout noise imager adopts readout architecture comprises a column amplifier, a comparator, and a 10 to 12-bit programmable column parallel Single-Slope ADC along with a global 12-bit current DAC, which is programmable to generate various slope of ramp signals with implemented timing schemes to suppress readout noise. The circuit blocks partition strategy is consisting of detector array and vertical scanner in array wafer stacked bonded with ASIC wafer, which includes RICA ISP, and imager sensor readout peripheral circuitry.

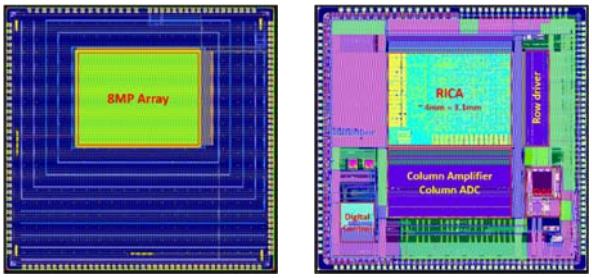


Figure 1. Stacked RICA ASIC wafer with Detector Array wafer of circuit partition.

RICA is an array of coarse-grain 16-bit arithmetic elements combined with an interconnect-fabric that allows building large data-paths, in a similar way to an FPGA. The programmable elements are heterogenous and selected to efficiently map imaging and video applications. Unlike an FPGA

where a single configuration is loaded, in this architecture a very wide Program RAM (PRAM) allows fast switching between several contexts. The switching is controlled by an element in the array called the JUMP-cell, which effectively acts as an instruction-controller; the address of the executed context is generated at run-time and is generally data-dependent. This gives the architecture the ability to easily execute the control part of the target algorithms and allows the high-level C compiler to directly map the program-flow as different contexts, in a similar way to DSPs. To efficiently map an algorithm onto the array, the compiler tries to make contexts utilize as many cells as possible by increasing their parallelism, in a similar way to ASIC and FPGA designs. The array is then clocked at the lowest frequency possible to achieve the required input/output bandwidth, which is usually around 100MHz. This massive parallelism gives RICA an unsurpassed advantage in saving power over running the same task on an Application Processor.

As seen in Fig. 2, a separate SBUFs block contains the data RAM. The RAM consists of 32 separate line-long 16-bit banks that can be accesses in parallel individually, giving a high internal data bandwidth to the core. The SBUF interfaces allow to easily create line-delays and image windows. The core supports a wide input/output, but for the purpose of stacked image sensor this was limited to a single pixel input and output.

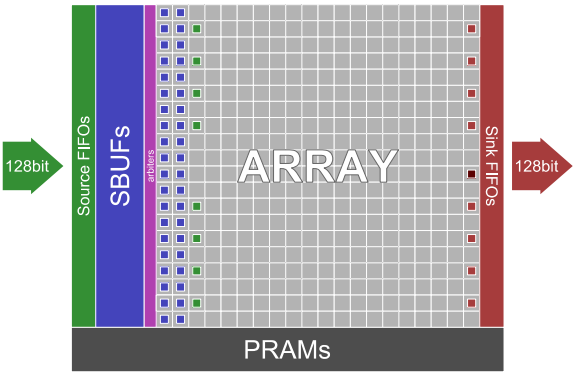


Figure 2. Graphic representation of Silicon layout for RICA core.

3. Device Characteristics

The device performance of the imager array features reasonable low dark current & hot pixel distribution, and linear full well capacity of 4800-e, with sense node conversion gain of 120uV/e, and sensitivity of 4200 e-lux-sec @530 nm. The read noise is measured at 8X analog gain, and input referred of 2.2-e_rms has been achieved. The photo-response characteristics, such as non-uniformity, non-linearity & blooming ratio, are pretty much intact as compared to the leading-edge CMOS imager solutions. Furthermore, the stacked image sensor performance is not degraded from its non-stacked imager counterpart, and in some cases, outperforms the BSI baseline. The summarized device key performance indices are listed in Table-1.

Performance Indices		1.1um
Dark Current @ 60 ºC	e/sec	5
Hot Pixel > 140-e/s	ppm	500
Read Noise	e	2.2
RTS @99.9%	e	7.2
FWC_linear	e	4800
Sensitivity @530nm	e/lux-s	4200
PRNU	%	0.7
PRNL	%	< 5
Blooming Ratio	%	<3
Image Lag	e	< 1
QE_max@530nm	%	73

Table 1. Device key performance indices measure

The spectral response curves of the 1.1um pixel device is illustrated in Fig. 3. Color Correction Matrix was extracted from the QE curves to achieve white balance & combat pixel cross-talk and color separation. We can also examine our de-mosaic algorithm robustness via RICA on mitigating the intrinsic cross-talk of small pixel, and maintain the trade-off balance between SNR and color error.

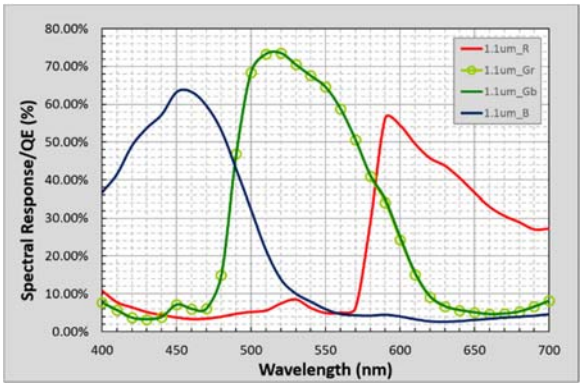


Figure 3. QE plot of detector array

4. Image Processing

Today's ISP arrangement via Application Processor is limited to supporting RGBG Bayer pattern. With new patterns of RGBW, RGBIR, zigzag-RGB, i-HDR, & PDAF, current solution is to perform the pre-processing in external chip, and converted it to RGBG Bayer. With our proposed RICA stacked solution, it provides flexibility to programmable image processing algorithms and allow enhancing image quality in different pixel array patterns & formats.

Our Universal De-mosaic algorithm [3] was applied to process the raw image data captured with the stacked imager, which illustrated superior image fidelity with PSNR of 40.7, 41.5, & 39 dB in Red/Green/Blue color channels respectively, which were averaged across 6-patch of Macbeth Color Chart. The final processed image is shown in Fig-4. In addition, performed de-mosaicking Bayer CFA pattern, other patterns including RGBW, Bayer 1.5X (3x3), Kodak PanChromatic, and Lukac (4x4) [4] CFA patterns all proven efficient with satisfactory PSNR & color fidelity.



Figure 4. Image after universal de-mosaic processing

In addition to the visible imaging applications, other use cases in the NIR sensing, including structured light depth sensing, 3D scanning, object recognition, & iris scanning. Illustrated in Fig-5 demonstrated a structured light depth sensing example of NIR raw data. The image was captured by a single mode edge emitter laser projector with embedded Diffractive Optical Element (DOE) pattern, and reflected from objects onto the NIR receiver focal plane followed by processing in RICA. The RICA processed code detection achieved depth map as shown in Fig-6.

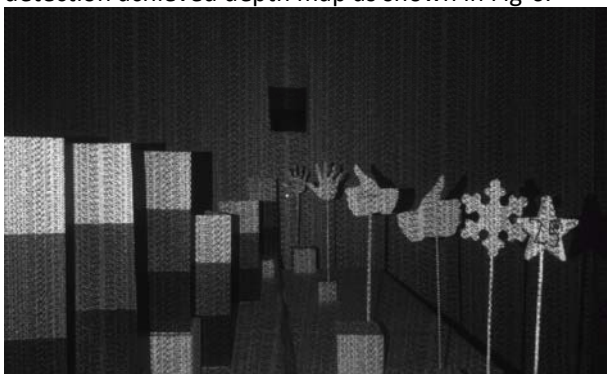


Figure 5. Raw NIR image with structured light DOE projector

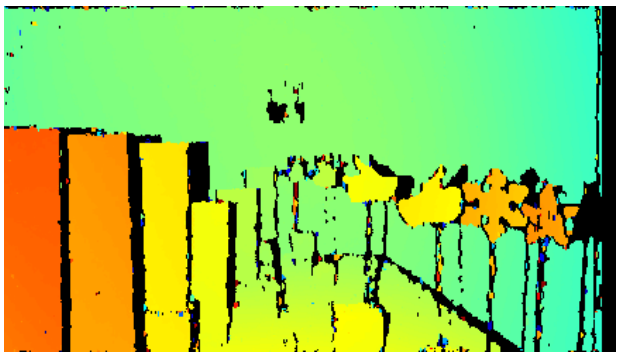


Figure 6. After code detection of Fig. 5 and depth map created

Furthermore, a 3D scanning was performed with the structured light projector, which collect a big data sets composed of 3D point data, and processed with RICA 3D Reconstruction algorithm in creating point cloud [5,6] image shown in Fig-7.

The demonstrated structured light depth sensing solution with RCIA stacked image sensor will enable future commercialization in outdoor point clouds for Light Detection And Ranging (LiDAR) to collect geographic point cloud data, and in autonomous driving applications.

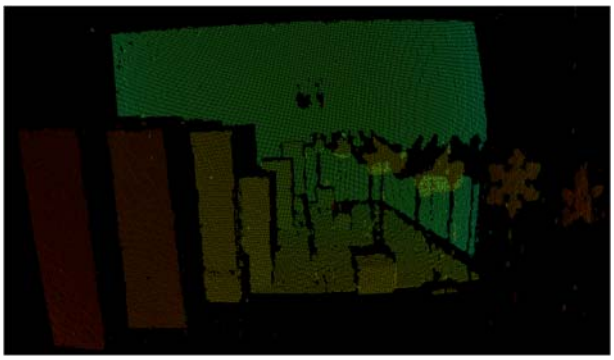


Figure 7. Point clouds created by 3D scanning with structured light DOE projector

5. Conclusion

We have successfully designed and prototyped a dedicated image signal processing engine stacked with an 8MP image array in 45nm CMOS BSI image sensor & 40nm ASIC technologies. The demonstrated stacked Sensor solution will provide flexible, power saving, and efficient programmable ISP engine to enable emergent digital imaging applications, and future computational photography.

6. References

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